PURIFI

# PURE SOUND

Building a Straight Wire
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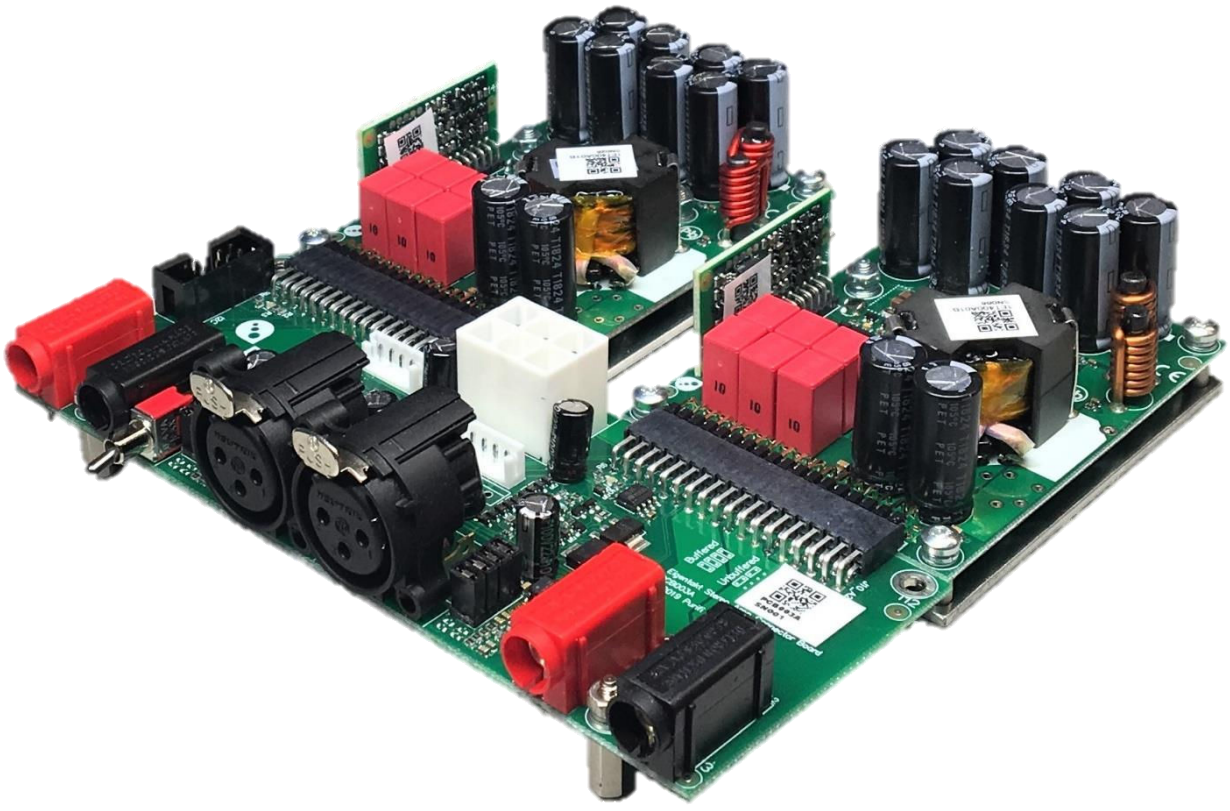
## EVAL1
# USER'S GUIDE



# 1 Introduction

This document describes the operation, function and usage of the EVAL1 evaluation kit ("EVM") consisting of two 1ET400A amplifier modules and one FE02 stereo front-end module.

## 1.1 Usage and Purpose

The EVM is provided for engineering evaluation and laboratory test purposes only. Great care should be taken when handling the EVM, especially when connected to power supplies and loads. Observe the voltage and power ratings and apply suitable precautions to protect the operator from electrical hazards.

Also note that the EVM is provided as an unshielded PCB assembly and should be protected from ESD as well as mechanical stress.

### 1.1.1 Setup and operation

1. Plug 1ET400A modules into the Front-End Board (FE02)
2. Place EVM on a flat surface Note that the amplifier base plates are connected to GND and should be attached to an external heatsink, e.g., a larger aluminum plate, for extended high power testing.
3. Connect external laboratory supplies (or other suitable PSU's) to FE02 (refer to section 4)
4. Connect audio inputs and speakers (or other suitable loads/test equipment)
5. Enable operation via toggle-switch on FE02
   Two red LED's will light up when all supply voltages are within operational range.
6. It is recommended to disable operation (toggle-switch) and turn off all power supplies when module is not in use

### 1.1.2 Power Testing

The amplifier modules are protected from overheat via individual thermal protection systems that monitor the temperature of the aluminium base plates. The aluminium plates provide limited cooling, likely adequate for full-power music as well as typical test sweeps etc., However, for continues high power delivery additional cooling is required.

## 2 EVAL1 Overview

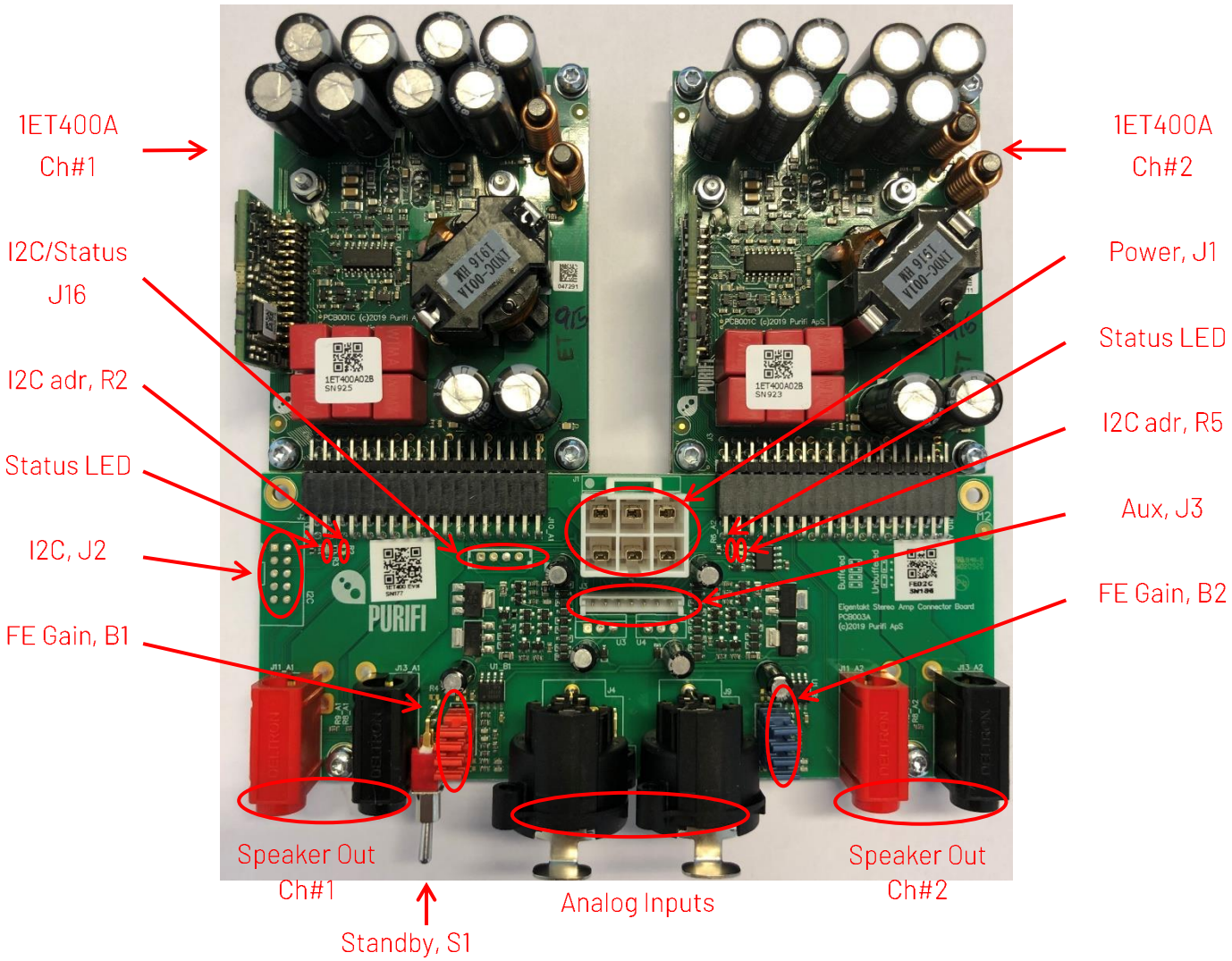



*Figure 1 EVAL1 Overview*

# 3 Interface

## 3.1 Standby switch, S1

| Position | Description |
|---|---|
| UP | Operational – Power stage is on |
| DOWN | Standby, Power stage is off |

*Table 1 Standby switch, S1*

## 3.2 Power connector, J1


| Pin | Signal | Rating | I/O | Description |
|---|---|---|---|---|
| 1 | VDR | | P | Gate Drive Supply, referenced to -VP |
| 2 | +VP | | P | Power Stage Supply, positive rail |
| 3,6 | GND | | - | Ground |
| 4,5 | -VP | | P | Power Stage Supply, negative rail |

*Table 2 Power connector, J1*

Connector type equivalent: JST: B06P-VL.
Matching cable part: JST: VLP-06V.

## 3.3 I2C connector, J2 (for e.g., Aardvark)


| Pin | Signal | Rating | I/O | Description |
|---|---|---|---|---|
| 1 | SCL | | I | I2C clock (SW Mode) |
| 2 | GND | | - | Ground |
| 3 | SDA | | I | I2C Data (SW Mode) |
| 10 | GND | | - | Ground |
| 4,5,6, 7,8,9 | NC | | - | Not connected |

*Table 3 I2C connector, J2 (for e.g., Aardvark)*

Note: J2 is per default not mounted
Connector: 2x5pin IDC header: T821110A1S100CEU Amphenol

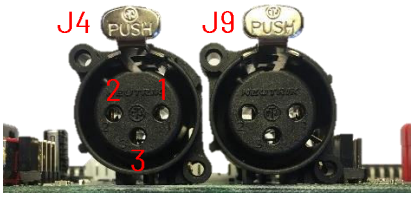
## 3.4 Aux connector, J3


| Pin | Signal | Rating | I/O | Description |
|---|---|---|---|---|
| 1 | PSUDIS<br>/AMPON | | O<br>I | PSU off control signal (SW Mode), or<br>Amplifier Disable (HW Mode) – *pull low to enable Amp* |
| 2 | SDA<br>READY | | I<br>O | I2C Data (SW Mode), or<br>Amplifier Ready (HW Mode) – "all good for operation" when high |
| 3 | SCL<br>/FATAL | | I<br>O | I2C clock (SW Mode), or<br>Amplifier "error/fail" (HW Mode) – *signal goes low on error* |
| 4 | +5V | | P | 5V output (from onboard regulator), 20mA max load. Requires R1 mounted |
| 5 | +VUNREG | | P | Voltage regulator input, positive rail |
| 6 | GND | | - | Ground |
| 7 | -VUNREG | | P | Voltage regulator input, negative rail |

*Table 4 Aux connector, J3*

Connector type: JST: B7B-EH-A(LF)(SN).
Matching cable part: JST: EHR-7.

## 3.5 Analog input XLR connectors, J4 & J9



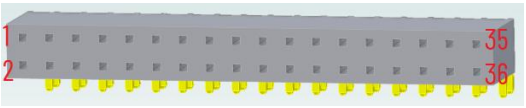

| Pin | Signal | Rating | I/O | Description |
|---|---|---|---|---|
| 1 | GND | | - | Ground |
| 2 | IN+ | | I | Analog input, positive |
| 3 | IN- | | I | Analog input, negative |

*Table 5 Analog input XLR connectors, J4 & J9*

Connector type: Neutrik NC3FAH2

If a single ended input is need then connect GND and IN- to the negative analog input.

## 3.6 Edge connectors, J10_A1 & J10_A2

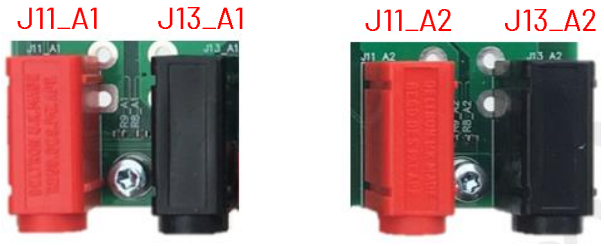



| Pin | Signal | Rating | I/O | Description |
|---|---|---|---|---|
| **Power Supplies** | | | | |
| 1, 2 | +VP | | P | Power Stage Supply, positive rail |
| 3,4,5 6,7,8 | GND | | - | Ground |
| 9,10 | -VP | | P | Power Stage Supply, negative rail |
| 11 | VDR | | P | Gate Drive Supply, referenced to -VP |
| 12 | VD | | P | (option use)External Voltage supply to on-board 3.3V regulator |
| 26 | +VOP | | P | OPAMPs, positive rail |
| 25 | -VOP | | P | OPAMPs, negative rail |
| 27 | GND | | - | Ground |
| **I/O's** | | | | |
| 13,14,15, 16,18 | OUT- | | O | Speaker Output, negative (internally connected to GND) |
| 17 | VFBLF- | | I | Feedback sense input, negative |
| 19 | VFBLF+ | | I | Feedback sense input, positive |
| 20,21,22, 23,24 | OUT+ | | O | Speaker Output, positive |
| 28,33,34 | NC | | - | Not connected |
| 29 | IN+ | | I | Analog Input, positive |
| 30 | IN- | | I | Analog Input, negative |
| 31 | HS/ADDR | | I | Mode/I2C Address Selection; set by one 1% resistor. |
| 32 | PSUDIS /AMPON | | O<br>I | PSU off control signal (SW Mode), or<br>Amplifier Disable (HW Mode)– *pull low to enable Amp* |
| 35 | SDA READY | | I<br>O | I2C Data (SW Mode), or<br>Amplifier Ready (HW Mode)– "all good for operation" when high |
| 36 | SCL /FATAL | | I<br>O | I2C clock (SW Mode), or<br>Amplifier "error/fail" (HW Mode)– *signal goes low on error* |

*Table 6 Edge Connector, J10_A1 & J10_A2*

Connector type: Samtec: SSW-118-02-T-D-RA

## 3.7 Speaker output connectors, J11 & J13



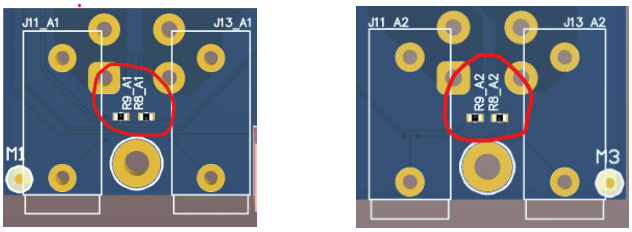

| Pin | Signal | Rating | I/O | Description |
|---|---|---|---|---|
| J11_A1 | OUT+ | | O | Speaker output, positive – Channel 1 |
| J13_A1 | OUT- | | O | Speaker output, negative – Channel 1 |
| J11_A2 | OUT+ | | O | Speaker output, positive – Channel 2 |
| J13_A2 | OUT- | | O | Speaker output, negative – Channel 2 |

*Table 7 Speaker output connectors, J11 & J13*

Connector: 4mm banana socket: Deltron: 571-0100(Black), 571-0500(Red)

Note:

The 1ET400A module senses directly at the speaker connector (VFBLF-, VFBLF+) to get lowest possible output impedance, so if the connectors J11 & J13 are removed there is a 1R 0603 resistor at position R8_A1, R9_A1 & R8_A2, R9_A2 to sense the output signal.




## 3.8 I2C/Status connector, J16


| Pin | Signal | Rating | I/O | Description |
|---|---|---|---|---|
| 1 | +5V | | P | 5V output (from onboard regulator), 20mA max load. Requires R1 mounted |
| 2 | SCL<br>/FATAL | 0 – 3,3V | I<br>O | I2C clock (SW Mode), or<br>Amplifier "error/fail" (HW Mode) – *signal goes low on error* |
| 3 | SDA<br>READY | 0 – 3,3V | I<br>O | I2C Data (SW Mode), or<br>Amplifier Ready (HW Mode) – "all good for operation" when high |
| 4 | GND | | - | Ground |

*Table 8 I2C/Status connector, J16*

Note: J16 is per default not mounted.

Connector type: JST: B4B-EH-A(LF)(SN).
Matching cable part: JST: EHR-4.

### 3.9 Gain/Bypass jumpers, B1 & B2

FE02 includes a ~13dB pre-gain stage for a total EVM gain of ~26dB. The pre-gain stage can be bypassed by location of two sets of jumpers:

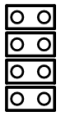
| Description | Pre-gain enabled | Pre-gain bypassed |
|---|---|---|
| Front-End gain | ~14dB | 0dB |
| Total EVM gain | ~27dB | ~13dB |
| Jumper setting |  |  |

*Table 9 Gain/Bypass jumpers, B1 & B2*

The pre-gain stage is made with a dual OPA1612 configured as Balanced/single-ended to balanced gain stage as shown below:

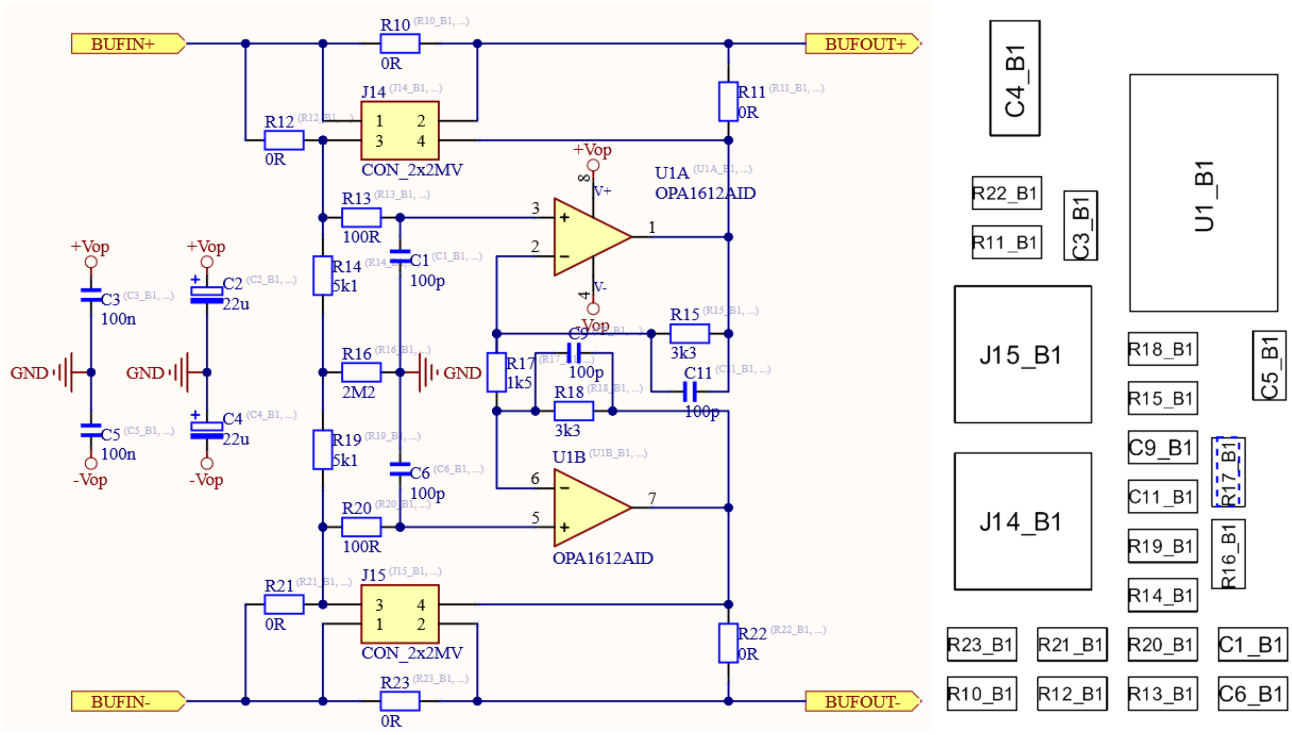



*Figure 2 Buffer Schematic*

Differential input impedance is 10.2kohm

The 0R resistors: R10, R11, R12, R21, R22, R23 are not mounted per default
The gain stage can be enabled/by-passed with the help of pin headed J14/J15 and jumpers as shown in Table 9.
If a fixed setting is needed the 0R resistors can be used as follows:

| Description | Pre-gain enabled | Pre-gain bypassed |
|---|---|---|
| Front-End gain | ~14dB | 0dB |
| Total EVM gain | ~27dB | ~13dB |
| Resistors mounted | R11, R12, R21, R22 | R10, R23 |
| Resistors NOT mounted | R10, R23 | R11, R12, R21, R22 |

*Table 10 Gain/Bypass resistors, B1 & B2*

If a different gain is needed resistor R17 can be modified.
Gain = 1+(R15+R18)/R17 = 1+(3.3K+3.3k)/1.5K = 5.4 = 14.6dB

# 4 Power Supplies

Refer to below figure showing required power supplies and how to connect these to FE02:

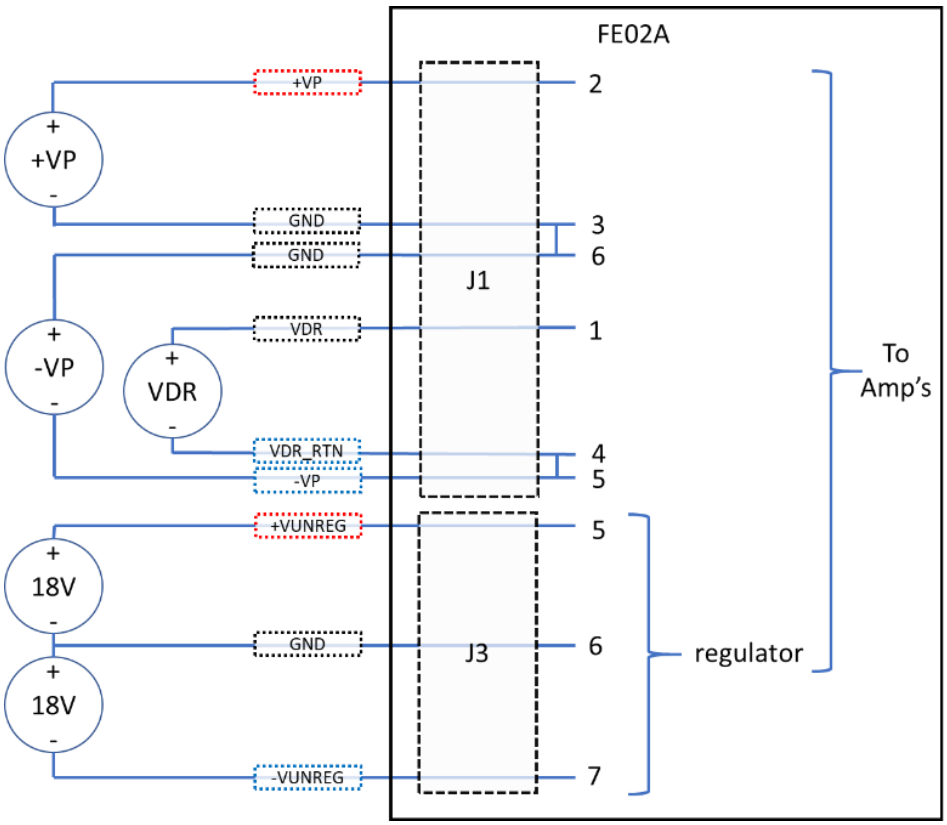



*Figure 3 Power Supplies*

All supplies levels should be crosschecked with the Recommended Operation Conditions as specified in the respective amplifier module data sheet.

Recommended supply voltages for EVAL1 (please also refer to the 1ET400A Data Sheet):

| Parameter | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Power Supplies | | | | | |
| +VP | Power Stage, positive rail voltage | 25 | 65 | 70 | V |
| -VP | Power Stage, negative rail voltage | -70 | -65 | -25 | V |
| VDR | Gate Drive, voltage (must be referenced to -VP) | 13.6 | 15 | 16.5 | V |
| +VUNREG | OPAMPs, positive rail voltage | 16.4 | 18 | 25 | V |
| -VUNREG | OPAMPs, negative rail voltage | -25 | -18 | -16.4 | V |

*Table 11 Recommended Supply Voltages*

## 4.1 Linear Regulators

FE02 includes two low noise discrete voltage regulators for the OPAMP's negative and positive supply voltages, +Vop & -Vop and a 5V regulator for the standby regulator, +VSBY. Schematic is shown here below:

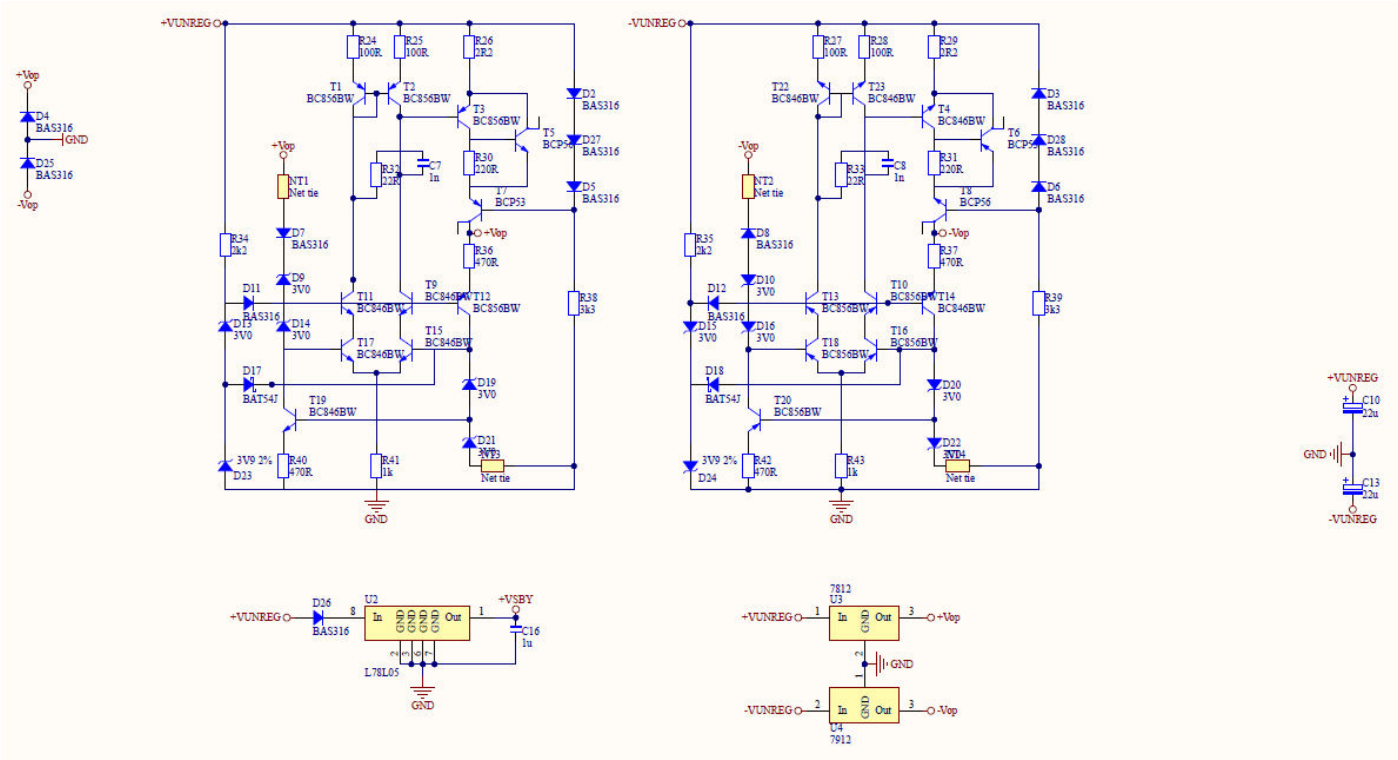



*Figure 4 Linear Regulator Schematic*

Note: U3 & U4 are not mounted

# 5 Operating Modes & Status Reporting

## 5.1 Mode Configuration

The EVAL1 can operate in two modes:

1. HW Mode: all control and status via pins (HW interface) – DEFAULT CONFIGUTATION
2. SW Mode: enables control and status via I2C interface

FE02 is configured for HW Mode by default. To reconfigure for SW Mode, at bit of soldering is required, see Table 12 and Figure 5:

| FP | Channel | Description | HW Mode | SW Mode |
|---|---|---|---|---|
| R6_A1 | 1 | Mode Selection | **Diode** | 0Ω shunt |
| R6_A2 | 2 | | | |
| R2 | 1 | I2C Address Selection | **open** | Refer to data sheet |
| R5 | 2 | | | |

*Table 12 Mode Selection*

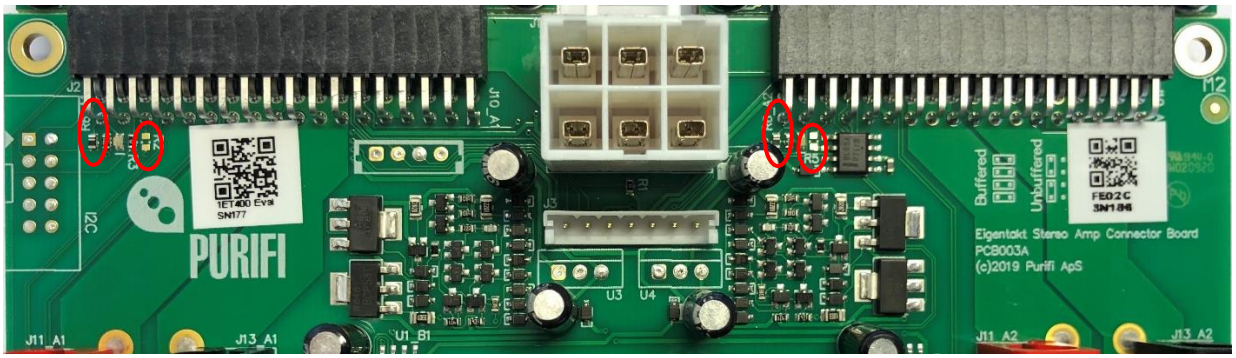



*Figure 5 Mode Selection*

## 5.2 HW Mode

The amplifier modules are controlled via toggle switch S1 connected to amplifier control signal /AMPON. /AMPON is also made available on connectors J3 and can be controlled via external source once shunt R3 has been removed.

Amplifier status is signaled via READY and /FATAL:

READY signals are connected to individual LED's on FE02. LED's are located close to pin 1 of the amplifier edge connectors.

/FATAL signals are wire or'ed together on FE02 and pinned out on connectors: J2, J3 and J16.

## 5.3 SW Model

The main feature of the SW Mode is access via I2C to status and control information. The I2C register map can be found in the amplifier data sheet.

I2C is accessed via SCL, SDA on connectors J2, J3 and J16.

The I2C address can be programmed via value of resistors R2 and R5 on FE02. Refer to the **Mode Selection via HS/ADR** table in the amplifier data sheet for information on resistor value vs. I2C address.

# 6 Mechanical Specifications & System Considerations

## 6.1 EVAL1 Dimensions

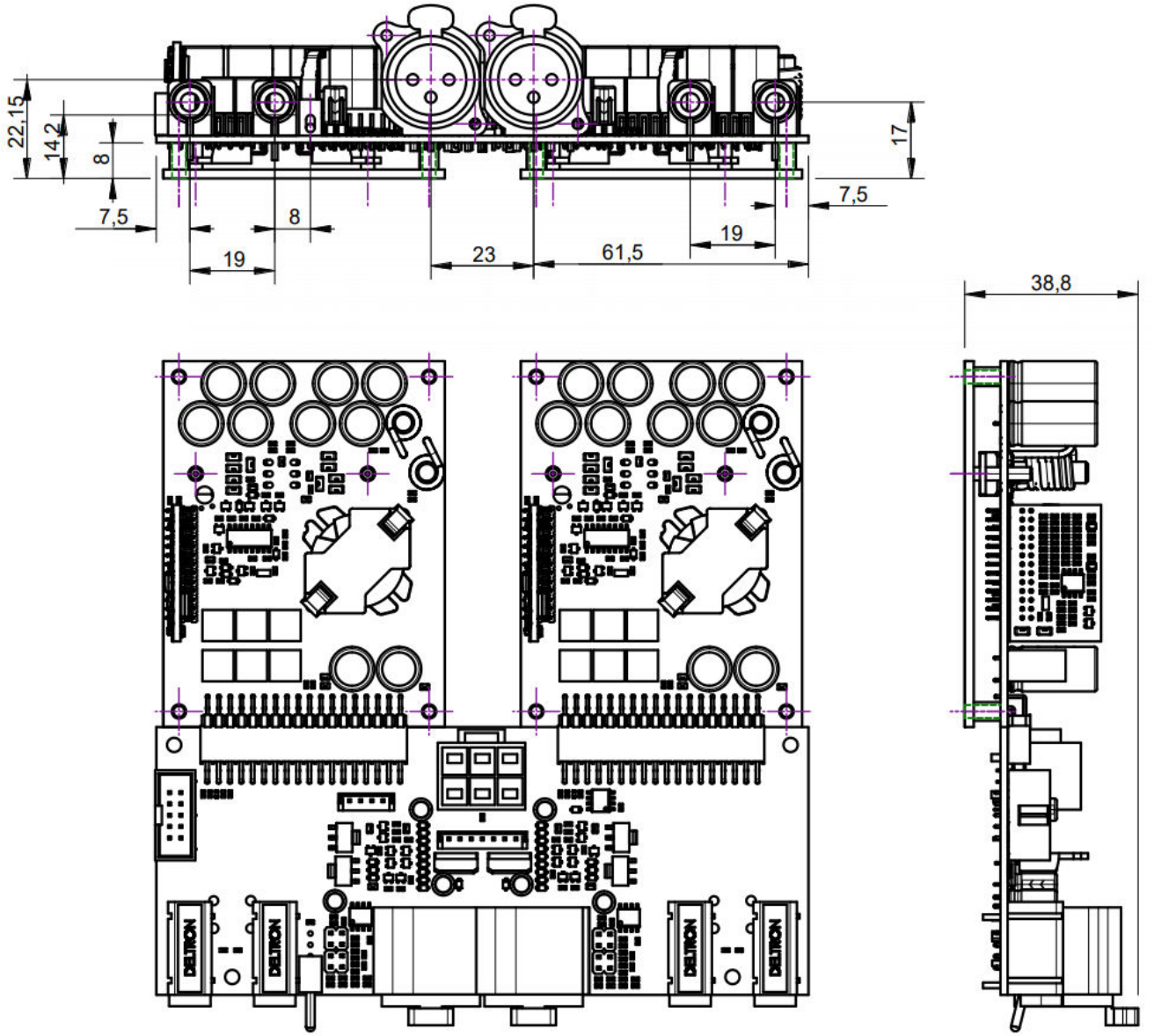



*Figure 6 Dimensions*

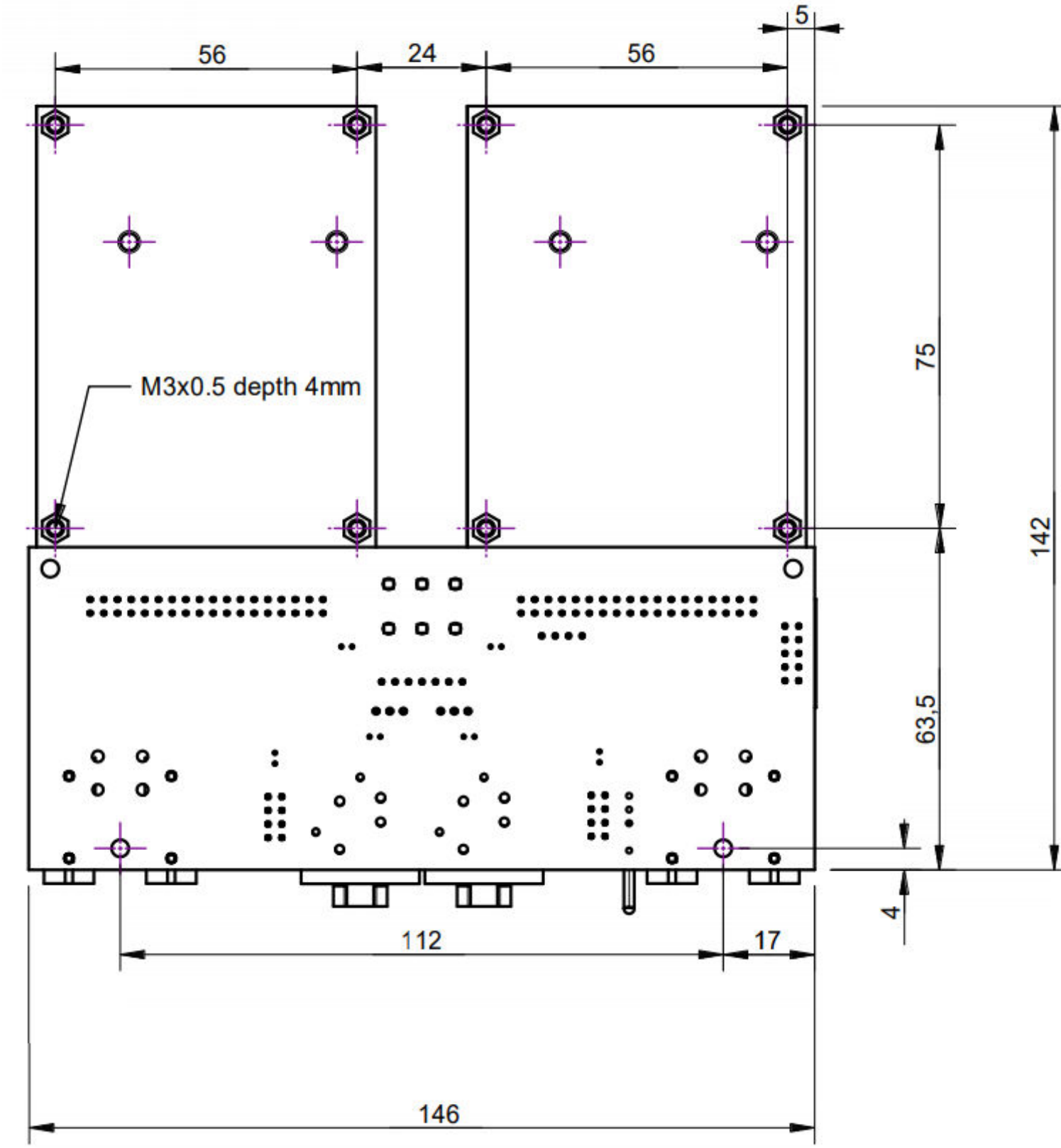



*Figure 7 Bottom-side mounting holes (scale 1:1 if printet on A4)*

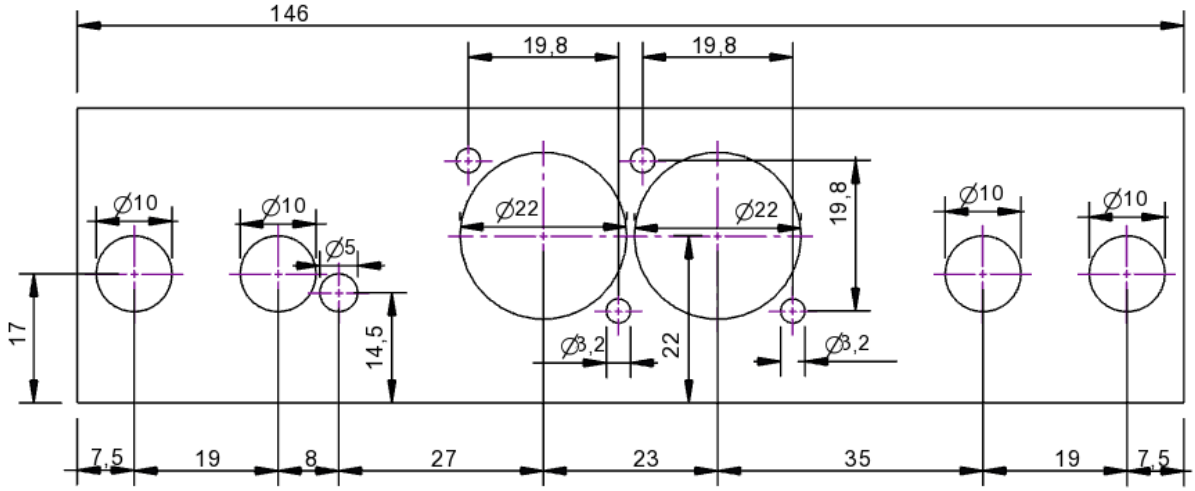



Figure 8 Back plate mounting holes (Scale 1:1 if printet on A4)

Note: Dimensions from bottom mounting plate including the 8mm standoff.

## 6.2 Thermal Requirements

While 1ET400A has very low idle losses and high overall efficiency, adequate cooling is essential for sustained power delivery. Careful considerations must be given to design of the thermal system in order to achieve desired output power specifications.

It is recommended to mount the module on a heatsink, e.g., an adequately design aluminum chassis.

## 6.3 Mechanical Requirements

Related to mechanical robustness of the end application: it is the reasonability of the system integrator to specify process, materials, locations, etc. for e.g., gluing of critical components which may be required and to prove/document short- and long-term performance and reliability. The system integrator must ensure integrity of mounting method and materials used related to fixation of the module. It is recommended to thoroughly test the final product for robustness against, e.g., shock and vibration.

## 6.4 Compliance Testing

1ET400A is designed with considerations for compliance of the end application. However, it is the responsibility of the system integrator to ensure any form of design-for-compliance and associated testing/certification which may be required. EVAL1 mounted in an adequate metal box has been tested to pass the EMI requirements.

# 7 External Standby Switch

Standby is controlled by the /AMPON signal, that is present on J3 pin-1. J3 also have a GND pin, so an external standby switch can be implemented by wiring a switch on J3 from Pin-1 to pin-6.

The revision C of the FE02 board in HW-mode comes with two diodes that OR the READY signal from Ch1 and C2, so a ON/OFF indication can be implemented by connecting a LED+330ohm resistor from J3 pin-2 to J3 pin-6.

The wiring diagram for this can look like shown below:

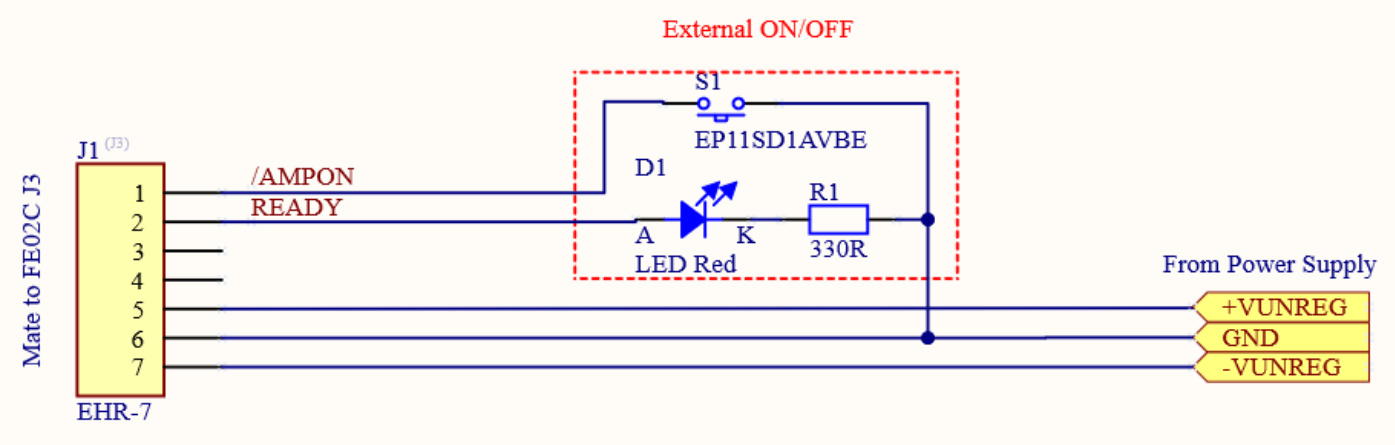



Figure 9 External ON/OFF Switch

# 8 Revision History

| Rev | Date | Description | ID |
|---|---|---|---|
| (0.92) | 2019-05 | Pre-release version (preliminary) | CNN |
| (1.00) | 2019-10 | Release version | CNN |
| (1.10) | 2020-01 | Added J10 pinout & schematic details | KNM |
| (1.20) | 2020-01 | Corrected gain equation in section 3.9, set +/-Vunreg max to 25V | KNM |
| (1.22) | 2020-01 | Added edge connector type & backplate mounting holes | KNM |
| (1.24) | 2020-07 | Updates to revC | KNM |
| (1.25) | 2020-09 | Corrected typo's | KNM |

*Table 13 Revision History*

1 EVM Use Restrictions and Warnings:

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